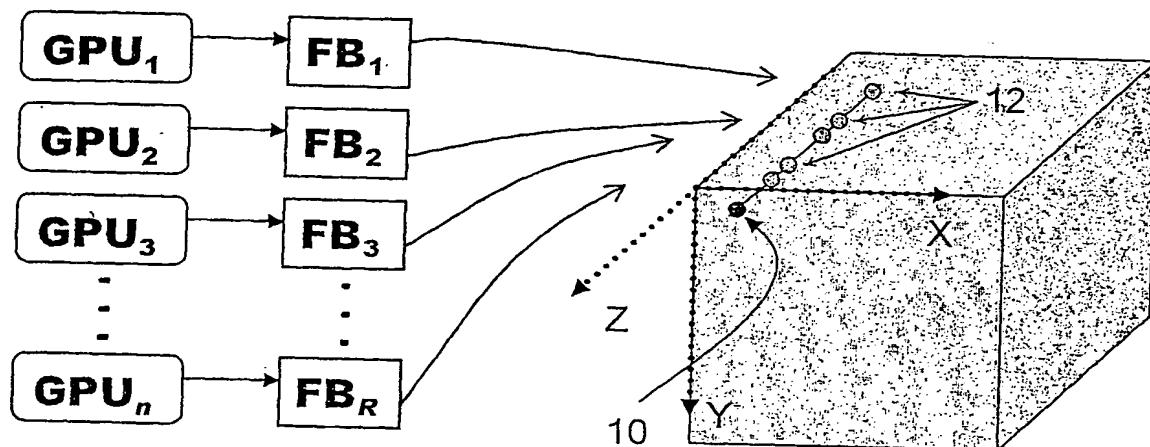
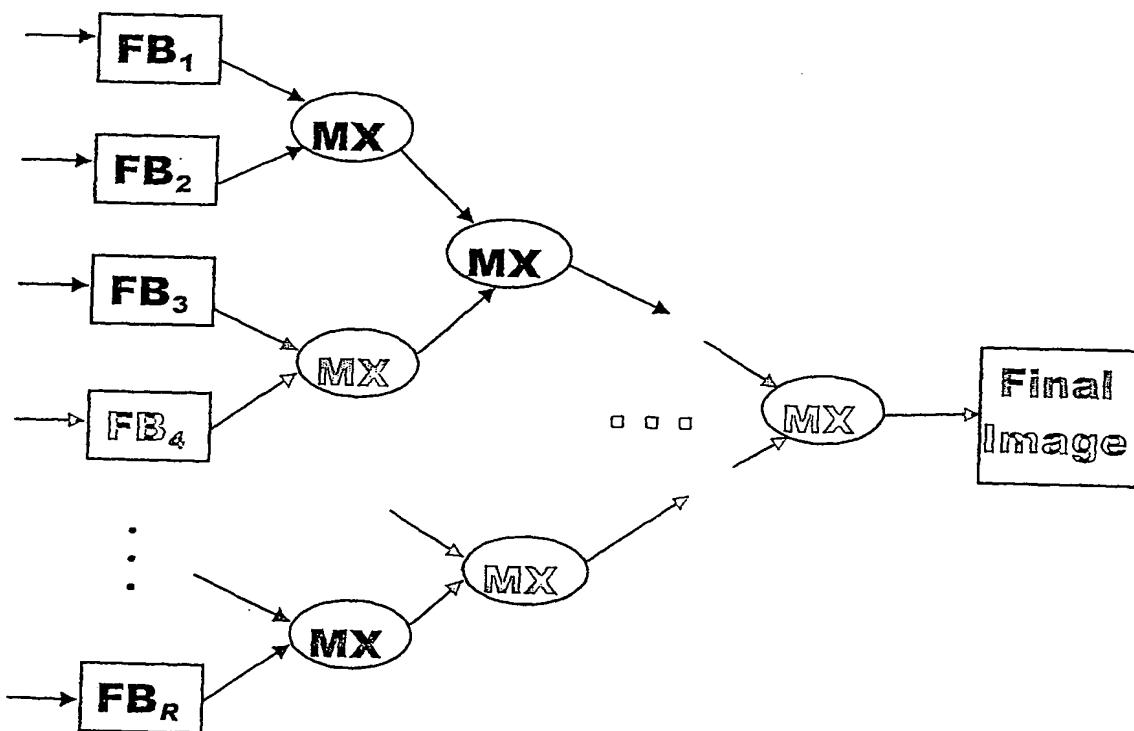


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*Fig. 1  
(Prior Art)*

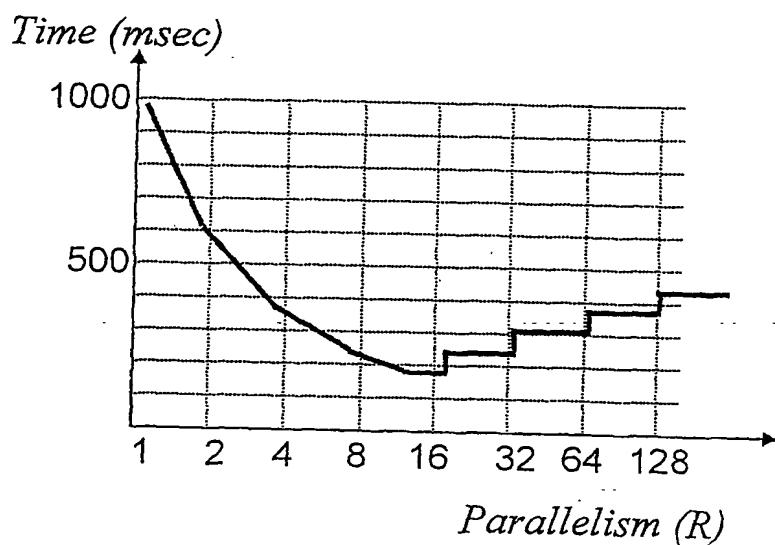


*Fig. 2A  
(Prior Art)*

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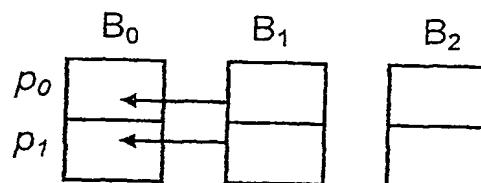
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*Fig. 2B  
(Prior Art)*

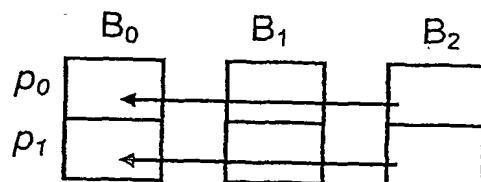


*Fig. 3A  
(Prior Art)*

Stage 1



Stage 2

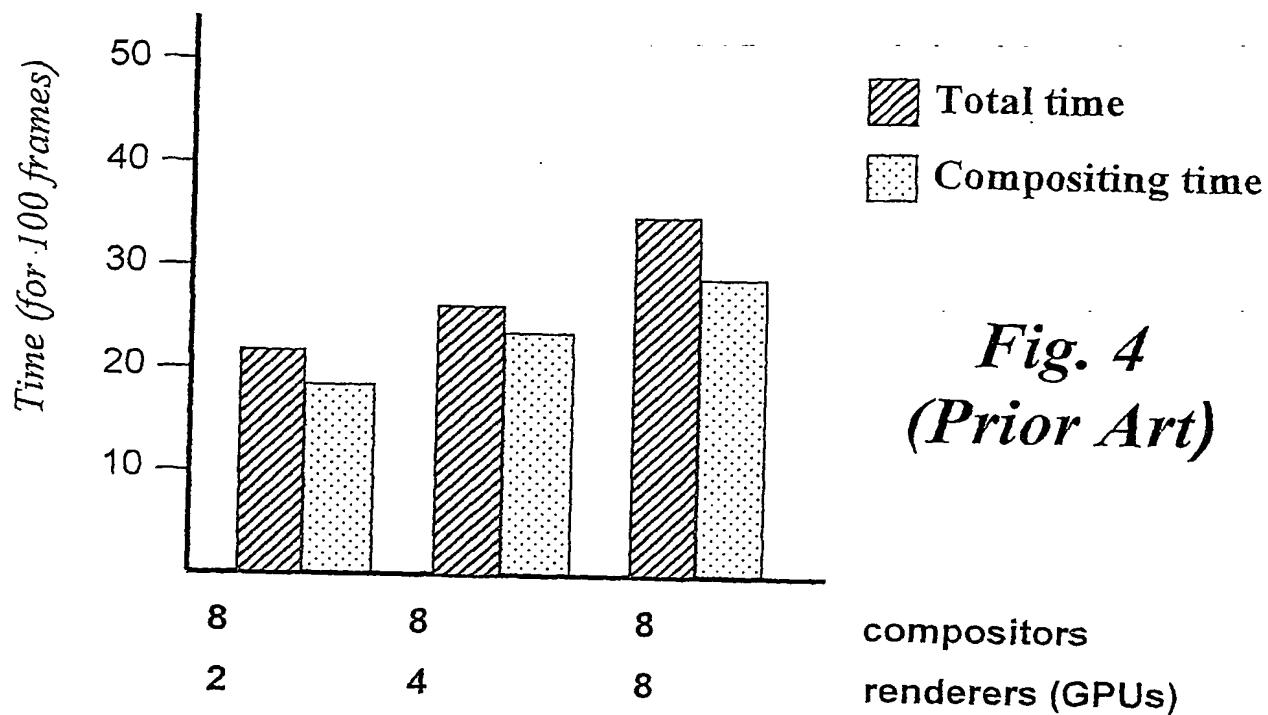


*Fig. 3B  
(Prior Art)*

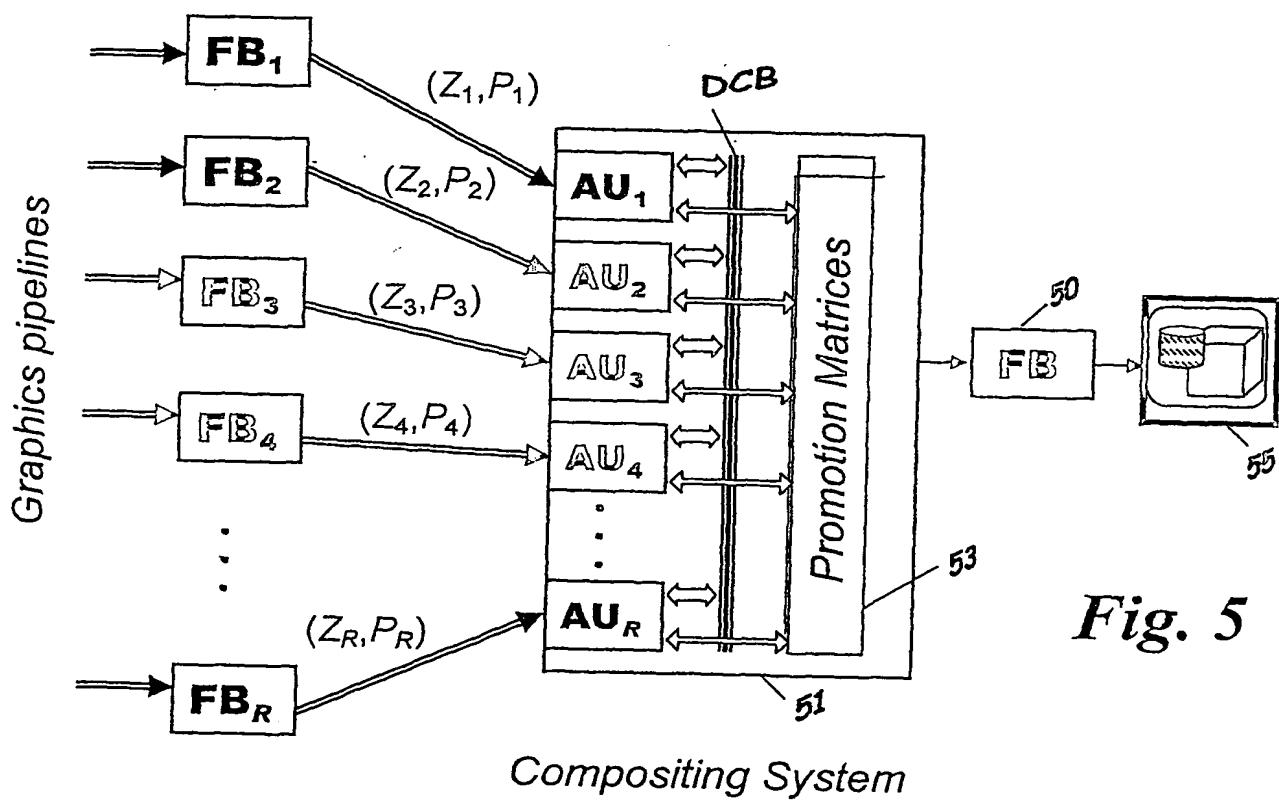
Do in parallel  
let  $B = \text{sub-image } i \text{ for processor } p_i$   
for  $n = 1, 2, 3, \dots, P$   
composite sub-images  $B_0$  and  $B_n$

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Compositing time for 1024 images.



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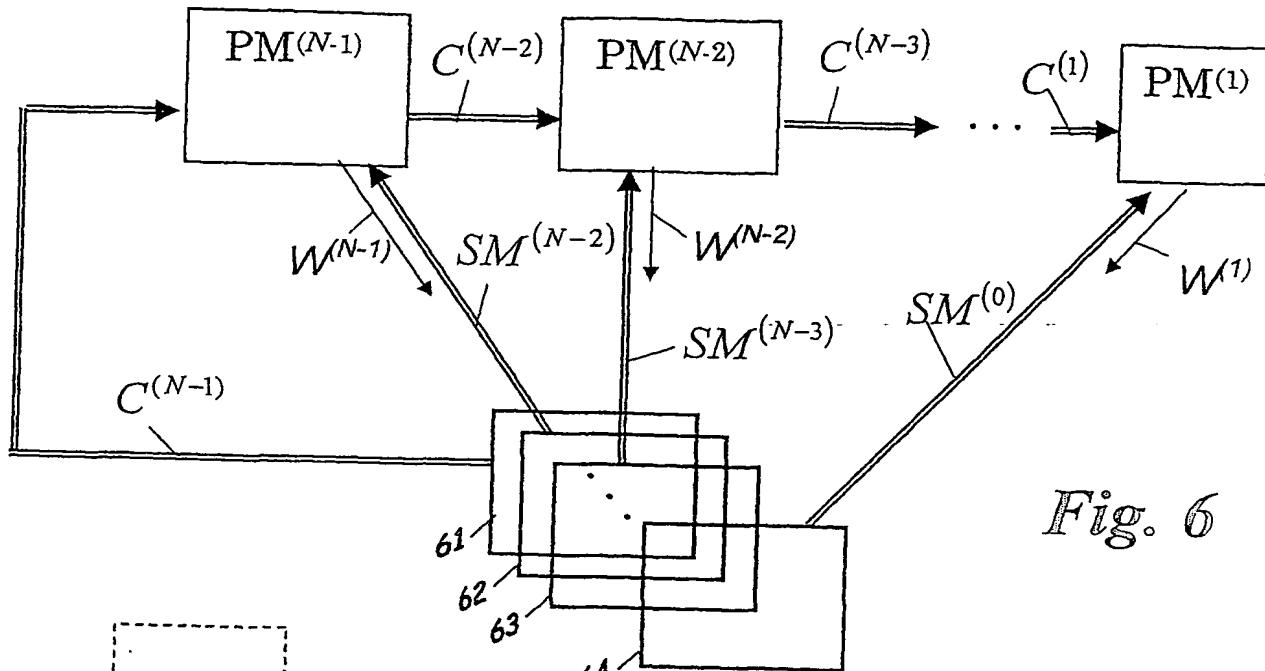


Fig. 6

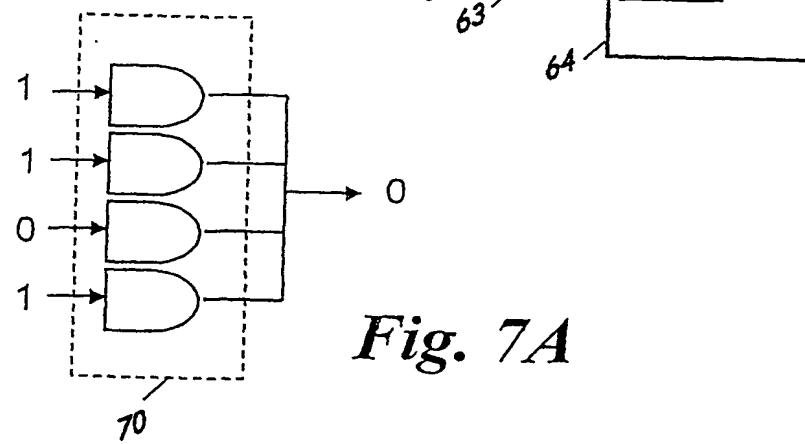


Fig. 7A

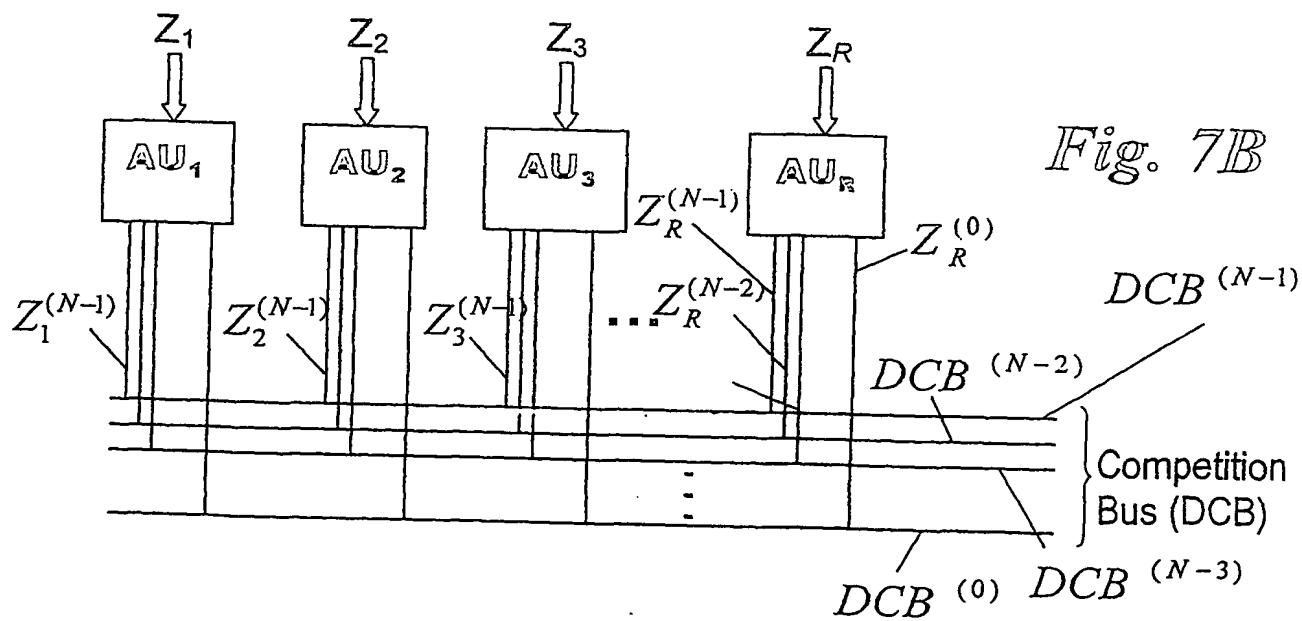
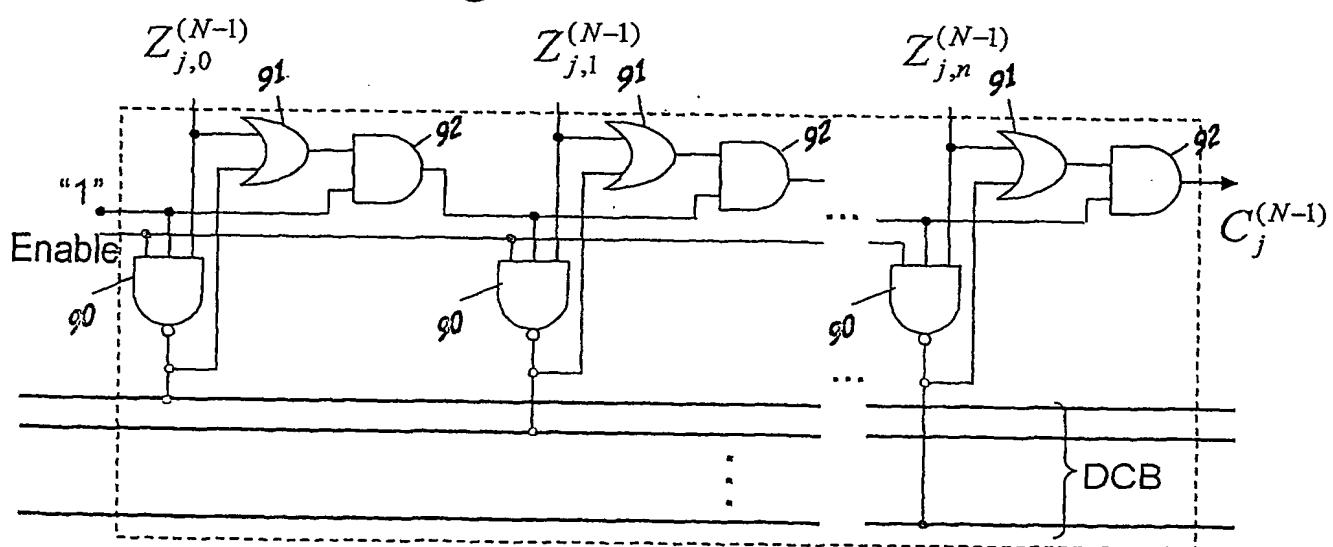
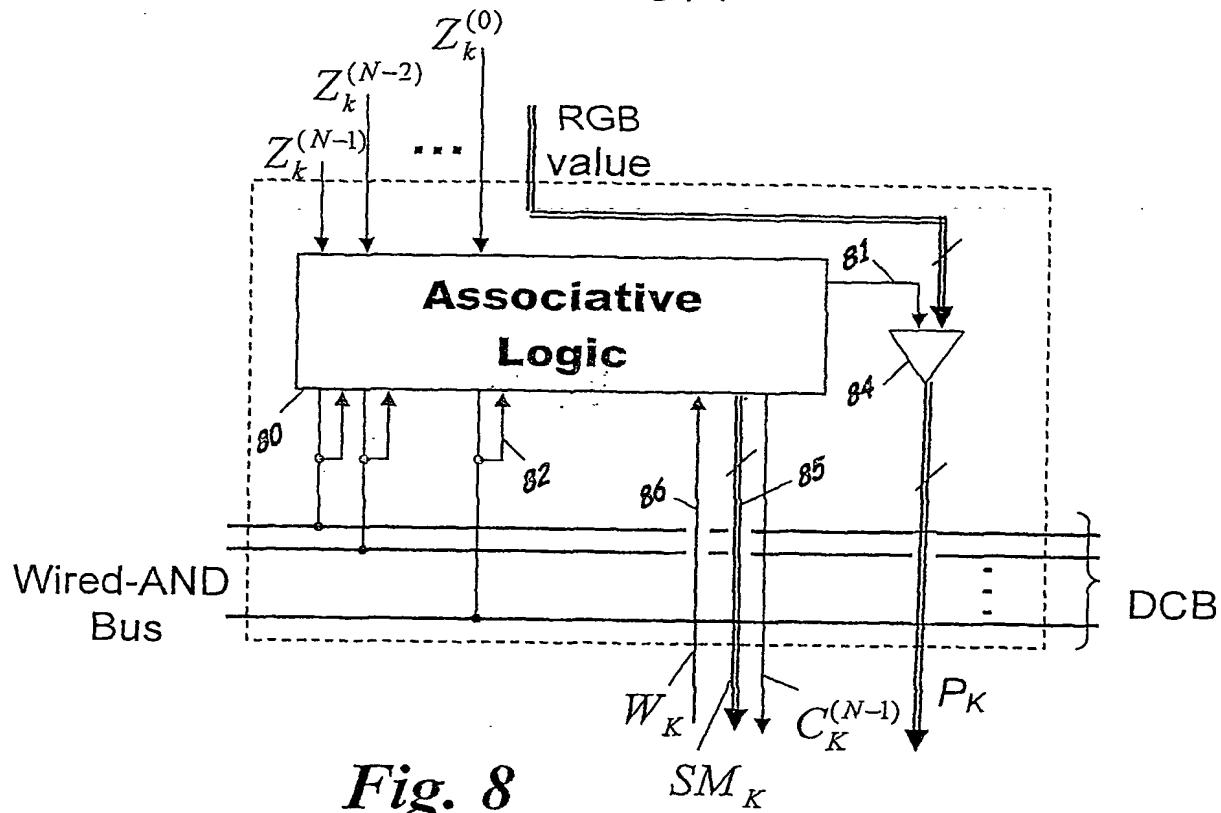


Fig. 7B

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From k-th rendering pipeline

**Fig. 9**

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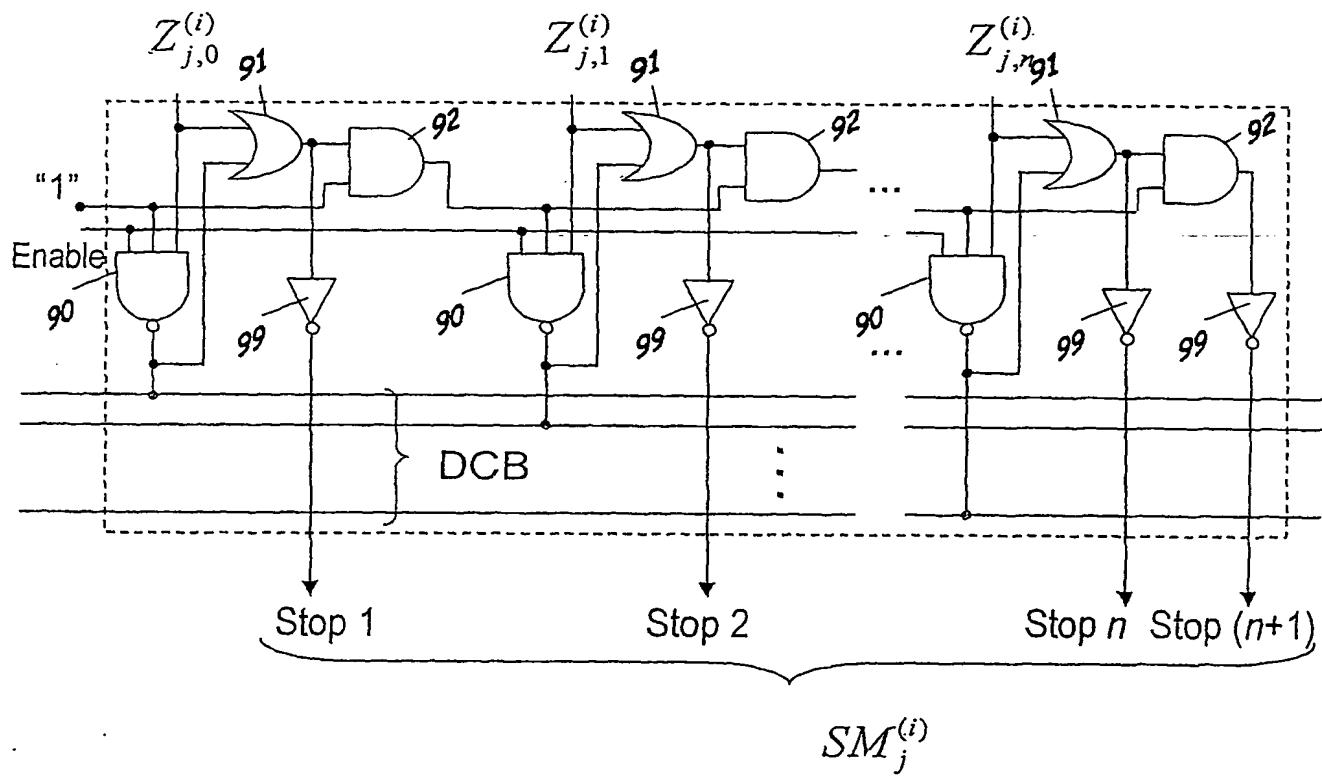
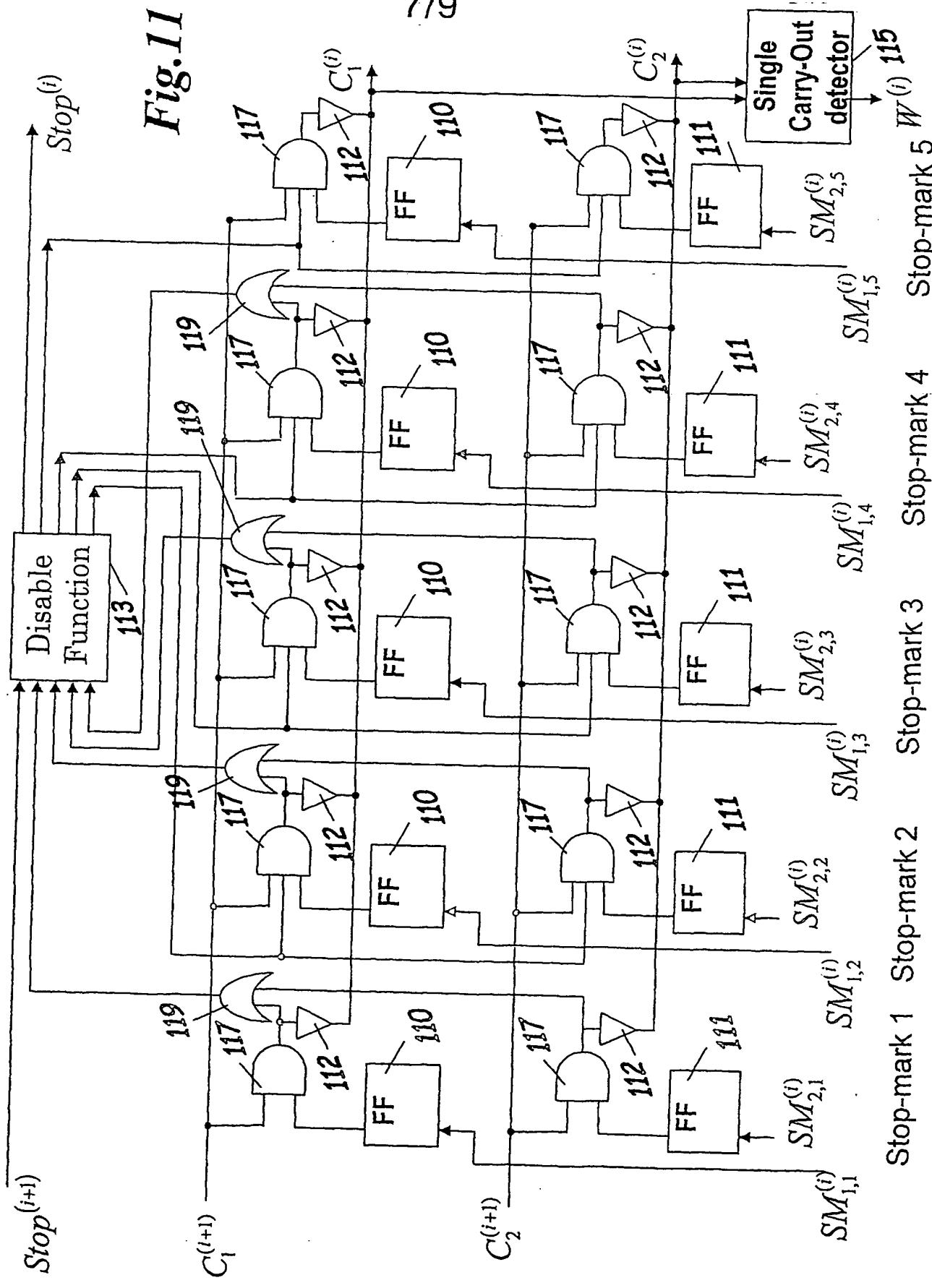


Fig. 10

Fig. 11

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Primary segment (8 bits) Carry-out(→) or stop	2 <sup>nd</sup> segment (8 bits) Carry-in, stop- mark, carry-out	3d segment (8 bits) Carry-in, stop- mark, carry-out	4th segment (8 bits) Carry-in, stop- mark, carry-out	Win
a stop	7	9		
b →	→ 9 →	→ 9 →	→ 8 →	15
c →	→ 8	9	7	
d stop	9	9	7	
e →	→ 9 →	→ 2	1	
Z <sub>1</sub> : 10001001	10101000	01000011	11111111	
Z <sub>2</sub> : 10101010	10101011	01000011	11111110	
Z <sub>3</sub> : 10101010	10101010	01000011	11111101	
Z <sub>4</sub> : 10101000	10101011	01000011	11111100	
Z <sub>5</sub> : 10101010	10101011	00111111	00000000	
	Z <sub>j</sub> <sup>(3)</sup>	Z <sub>j</sub> <sup>(2)</sup>	Z <sub>j</sub> <sup>(1)</sup>	Z <sub>j</sub> <sup>(0)</sup>

Fig. 12

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## Stack of SIUs

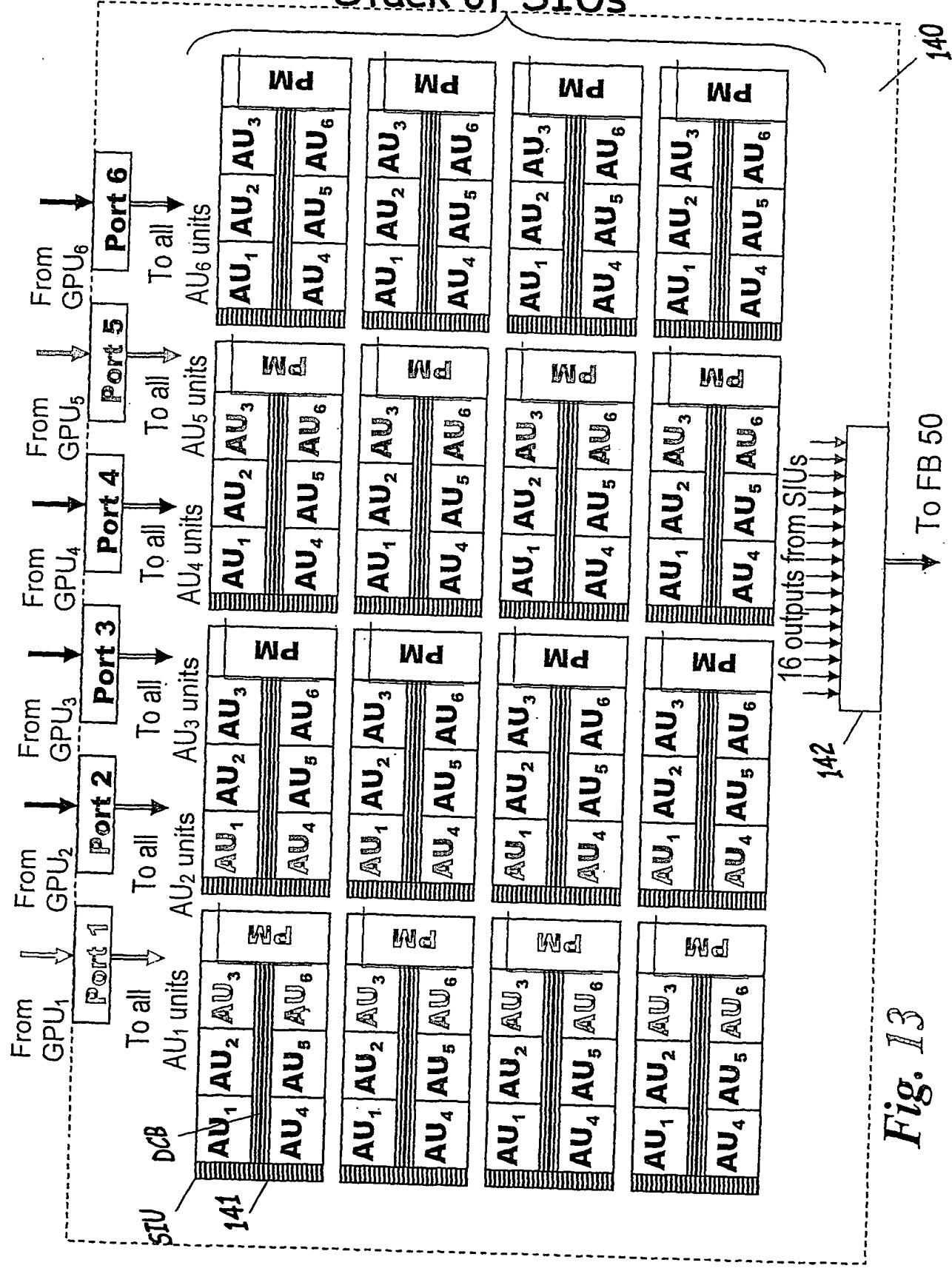


Fig. 13